LISTING OF CLAIMS:

1. (Currently Amended) A method for testing the error handling capabilities of a system's firmware by allowing an analyzer to trigger on a specific system event, comprising:

defining a specific system event to be monitored;

creating a trigger configured ~~in the analyzer, wherein the trigger is used~~ to allow [[the]] an analyzer to capture information related to the specific system event, wherein the trigger is controlled by an intelligent triggering controller external to the analyzer; and

receiving a signal at the analyzer from the intelligent triggering controller, wherein the signal automatically triggers the analyzer to capture and store a predetermined amount of data related to the specific system event before and after the trigger is executed.

2. (Currently Amended) The method of claim 1, wherein the ~~signal is sent from~~ intelligent triggering controller is one of a host system, a storage device, or a peer communications device.

3. (Currently Amended) The method of claim 2, wherein the ~~signal is sent from~~ intelligent triggering controller is a fibre channel host bus adapter in the host system.

4. (Original) The method of claim 1, wherein the analyzer is triggered within a millisecond of when the specific system event occurs.

5. (Currently Amended) The method of claim [[1]] 3, wherein the ~~specific system event is an error~~ fibre channel host bus adapter in the host system maps all connected devices logically to determine status conditions of the connected devices.

6. (Currently Amended) The method of claim 1, wherein the intelligent triggering controller controls the trigger in the analyzer to capture and store data regarding internal states of the system's firmware ~~analyzer is an FC analyzer~~.

7. (Currently Amended) The method of claim [[1]] 2, wherein the storage device includes initiators, targets, switches, or fabrics.

8. (Original) The method of claim 3, wherein the fibre channel host bus adapter includes a number of output pins, and wherein each output pin may be programmed with a separate triggering mechanism.

9. (Original) The method of claim 8, wherein the separate triggering mechanisms include detection of device errors above a certain threshold, device going away, illegal device activity, and input/output status.

10. (Currently Amended) A data processing system for testing the error handling capabilities of a system's firmware by allowing an analyzer to trigger on a specific system event, comprising:

defining means for defining a specific system event to be monitored;

creating means for creating a trigger configured ~~in the analyzer, wherein the trigger is used~~ to allow [[the]] an analyzer to capture information related to the specific system event, wherein the trigger is controlled by an intelligent triggering controller external to the analyzer; and

receiving means for receiving a signal at the analyzer from the intelligent triggering controller, wherein the signal automatically triggers the analyzer to capture and store a predetermined amount of data related to the specific system event before and after the trigger is executed.

11. (Currently Amended) The data processing system of claim 10, wherein the ~~signal is sent from~~ intelligent triggering controller is one of a host system, a storage device, or a peer communications device.

12. (Currently Amended) The data processing system of claim 11, wherein the ~~signal is sent from~~ intelligent triggering controller is a fibre channel host bus adapter in the host system.

13. (Original) The data processing system of claim 10, wherein the analyzer is triggered within a millisecond of when the specific system event occurs.

14. (Currently Amended) The data processing system of claim [[10]] 12, wherein the ~~specific system event is an error~~ fibre channel host bus adapter in the host system maps all connected devices logically to determine status conditions of the connected devices.

15. (Currently Amended) The data processing system of claim 10, wherein the intelligent triggering controller controls the trigger in the analyzer to capture and store data regarding internal states of the system's firmware ~~analyzer is an FC analyzer~~.

16. (Currently Amended) The data processing system of claim [[10]] 11, wherein the storage device includes initiators, targets, switches, or fabrics.

17. (Original) The data processing system of claim 12, wherein the fibre channel host bus adapter includes a number of output pins, and wherein each output pin may be programmed with a separate triggering mechanism.

18. (Original) The data processing system of claim 17, wherein the separate triggering mechanisms include detection of device errors above a certain threshold, device going away, illegal device activity, and input/output status.

19. (Currently Amended) A computer program product in a computer readable medium for testing the error handling capabilities of a system's firmware by allowing an analyzer to trigger on a specific system event, comprising:

first instructions for defining a specific system event to be monitored;

second instructions for creating a trigger configured ~~in the analyzer, wherein the trigger is used~~ to allow [[the]] an analyzer to capture information related to the specific system event, wherein the trigger is controlled by an intelligent triggering controller external to the analyzer; and

third instructions for receiving a signal at the analyzer, wherein the signal automatically triggers the analyzer to capture and store a predetermined amount of data related to the specific system event before and after the trigger is executed.

20. (Currently Amended) The computer program product of claim 19, wherein the ~~signal is sent from~~ intelligent triggering controller is one of a host system, a storage device, or a peer communications device.

21. (Currently Amended) The computer program product of claim 20, wherein the ~~signal is sent from~~ intelligent triggering controller is a fibre channel host bus adapter in the host system.

22. (Original) The computer program product of claim 19, wherein the analyzer is triggered within a millisecond of when the specific system event occurs.

23. (Currently Amended) The computer program product of claim [[19]] 21, wherein the ~~specific system event is an error~~ fibre channel host bus adapter in the host system maps all connected devices logically to determine status conditions of the connected devices.

24. (Currently Amended) The computer program product of claim 19, wherein the intelligent triggering controller controls the trigger in the analyzer to capture and store data regarding internal states of the system's firmware ~~analyzer is an FC analyzer~~.

25. (Currently Amended) The computer program product of claim [[19]] 20, wherein the storage device includes initiators, targets, switches, or fabrics.

26. (Original) The computer program product of claim 21, wherein the fibre channel host bus adapter includes a number of output pins, and wherein each output pin may be programmed with a separate triggering mechanism.

27. (Original) The computer program product of claim 26, wherein the separate triggering mechanisms include detection of device errors above a certain threshold, device going away, illegal device activity, and input/output status.